ABSTRACT OF THE DISCLOSURE

A system architecture for facilitating wireless communications includes a processor configured to implement interference avoidance processing and interference control processing for one or more groups of devices of a packet-communications system. The interference avoidance processing provides different addresses and a common clock for each of the groups of devices to minimize a frequency collision probability for the devices. The interference control processing detects when a same frequency element is selected for more than one of the devices for a same time slot and implements rescue processing to save data packets that are going to collide from being lost. In a preferred embodiment, the interference avoidance processing includes choosing particular address bits to provide the different addresses. In a preferred embodiment, the rescue processing is performed in consideration of a packet importance indicator which relates to one or more of: packet type, service type, a fairness criterion, and a history of prior connections made.